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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/719,218 | 11/20/2003 | Wen-Chou Vincent Wang | ALTRP100/A1198 | 3208 |

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BEYER WEAVER & THOMAS, LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

| EXAMINER | |
|---|---|
| RAO, SHRINIVAS H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/719,218 | WANG ET AL. | |
| | Examiner | Art Unit | |
| | Steven H. Rao | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *17-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## ***DETAILED ACTION***

### *Priority*

The Application as currently filed does not claim priority from any previously filed Patent Application. Therefore , currently the earliest available filing date is the U.S. filling date namely November 20, 2003.

### *Election/Restrictions*

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-16 are, drawn to a semiconductor package, classified in class 257, subclass 643.

II. Claims 17 to 34 , are drawn to a method pf forming a semiconductor package, classified in class 438, subclass 780 +.

Inventions Gr. I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)).

In the instant case the process as claimed can be used to make other and materially different product namely a semiconductor package other than wire bonding .

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Jeffery Weaver (31,314 ) on August 23, 2005 a provisional election was made without traverse to prosecute the invention of Gr. I, claims 1-16.

Affirmation of this election must be made by applicant in replying to this Office action.

Claims 17 to 34 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

***Information Disclosure Statement***

To date no IDS has been filed in this Application.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 16 are rejected under 35 U.S.C. 102(b) as being unpatentable over DiStefano . ( U.S. Patent No. 6,127,724, herein after DiStefano).

With respect to claim 1 DiStefano describes a semiconductor package comprising a die having a plurality of layers of low-K dielectric material, ( DiStefano figure 7 # 432-die) the die having a top surface, a bottom surface, and a plurality of side surfaces, each surface having associated corner and edge regions; ( DiStefano figure 7, etc.) a wire bonding packaging substrate having a plurality of electrical contacts, ( DiStefano figure 7 # 440 ) the packaging substrate being positioned under the die ( DiStefano figure 7 shaded portion under 432) ; a plurality of interconnects electrically connecting the die to the plurality of electrical contacts, ( DIStefano figure 7 # leads not numberes similar to flexible leads 54 in figure 3 ) a molding interface material applied to at least a portion of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die; ( DiStefano figure 7, col. 13 lines 55 to 65) and a molding cap covering at least a portion of the die, packaging substrate, interconnects, and molding interface material. ( DiStefano , figure 7 # 459).

With respect to claim 2 DiSteano describes a semiconductor package as recited in claim 1, wherein the molding interface material controls by applying compressive stress to the die, ( it is inherent that the same material disclosed by DiStefano as that claimed by Applicants' will recite the same compressive stress as claimed herein ) thereby strengthening the die against the at least one of tensile and shear stresses. ( it is further inherent that increase in one kind of

stress ( comrpesssive ) will reduce the other ( tensile and /or shear )stress thereby strengthening die against the at least one of tensile and shear stresses

The recitation, "wherein the molding interface material controls by applying compressive stress to the die, thereby strengthening the die against the at least one of tensile and shear stresses " is taken to be a hybrid functional and product by process recitation for which patentable weight cannot be given.

With respect to claim 3 DiStefano describes a semiconductor package as recited in claim 1, wherein the molding interface material is polyimide. ( DiStefano col. 8 lines 9 to 16) .

With respect to claim 4 Di Stefano describes a semiconductor package as recited in claim 3, wherein the molding interface material is on at least a portion of the plurality of side surfaces of the die. ( Di Stefano figure 7 encapsulant 458 on sides of 432).

With respect to claim 5 Di Stefano describes a semiconductor package as recited in claim 4, wherein the molding adjacent portion of the packaging interface material is also on a corresponding substrate such that the die is firmly attached to the packaging substrate. ( DiStefano figure 7).

The limitation " firmly attached " is also taken to be a product by process limitation for which no patentable weight can be given. See discussion above under claim 2 ( incorporated here by reference ) .

With respect to claim 6 Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material is applied in multiple non-contiguous regions to the top surface of the die. ( DiStafano figure 7) .

The limitation "is applied " is also taken to be a product by process limitation for which no patentable weight can be given. See discussion above under claim 2 ( incorporated here by reference ).

With respect to claim 7 Di Stefano describes a semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is rectangular in shape. ( DiStafano figure 7)

With respect to claim 8 Di Stefano describes a semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is triangular in shape. ( DiStafano figure 7)

With respect to claims 9 Di Stefano describes a semiconductor package as recited in claim 6, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns. Claim 9 depends from claim 6 and the product by process limitation not being given patentable weight in claim 6 is also applicable here.

With respect to claims 10 and 12, 11Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material is a contiguous region on the top surface of the die excluding corner regions. ( DiStafano figure 7)With respect to claim 11 Di Stefano describes a semiconductor package as recited in claim 10, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns.

With respect to claim 13 Di Stefano describes a semiconductor package as recited in claim 12, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns. ( rejected for same reasons as claim 11)

With respect to claim 14 Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material has a coefficient of thermal expansion between 5 ppm and 40 ppm. ( DiStefano col. 8 lines 17-40, col. 9 lines 18 to 65).

With respect to claim 15 Di Stefano describes a semiconductor package as recited in claim 14, wherein the molding interface material is over a substantial portion of the die such that a stress buffer zone is established between the die and the molding cap. ( figure 7 , col. 13 lines 53-62).

With respect to claim 16 Di Stefano describes a semiconductor package as recited in claim 1, wherein the plurality of layers includes extra low-K dielectric material. ( Di Stefano col. 6 line 39-polyimide known in the art to be low k-dielctric material ).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is ( 571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

LONG PHAM
PRIMARY EXAMINER

over

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

September 16, 2005.

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